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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NHU, DAVID	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,477	MITANI ET AL.	
	Examiner	Art Unit	
	David Nhu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *1-11 and 14-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12,13 and 19-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4*.
4)☐ Interview Summary (PTO-413) Paper No(s) _____.
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other:

DETAILED ACTIONS

Election/Restrictions

1. Applicant's election of Species I (Claims 12-13, 19-32) in page No. 9 is acknowledge. Claims 12-13, 19-32 are remained for examination. Claims 14-18 are withdrawn from consideration as being directed to non-election invention. See 37 CFR 1.142 (b) and MPEP & 821.03.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 12-13, 19-23, 31-32 are rejected under U.S.C 103(a) as being unpatentable over Numata et al (6,043,536) in view of Masuda (6,063,686).

Regarding claim 12, Numata, figures 1-51, and related text on col. 1-30, (figures 1, 44), disclose a method of driving a semiconductor device having a field effect transistor (FET) 1 formed in a semiconductor layer provided on an insulating layer 3, a body electrode 6 electrically connected to a channel 4 forming region of said TFT, and a back gate electrode 11 provided below the insulating layer 3 in an opposing relationship to the channel forming region of said TFT.

It is noted that Numata fails to teach the step of applying a potential lying in a direction to induce an electrical charge of conduction type opposite to a channel formed in a surface layer

of the channel forming region of said TFT, in a lower portion of the channel forming region thereof to said body electrode and said back gate electrode or at least said back gate electrode so as to increase a threshold voltage of said TFT.

However, Masuda, figures 1-44, and related text on col. 1-30, (figures 1-10), teach the step of applying a potential lying in a direction to induce an electrical charge of conduction type opposite to a channel formed in a surface layer of the channel forming region of said TFT, in a lower portion of the channel forming region thereof to said body electrode and said back gate electrode or at least said back gate electrode so as to increase a threshold voltage of said TFT.

Regarding claim 13, Numata, figures 1-51, and related text on col. 1-30, (figures 1, 44), disclose a method of driving a semiconductor device having a field effect transistor (FET) 1 formed in a semiconductor layer provided on an insulating layer 3, a body electrode 6 electrically connected to a channel 4 forming region of said TFT, and a back gate electrode 11 provided below the insulating layer 3 in an opposing relationship to the channel forming region of said TFT.

It is noted that Numata fails to teach the step of applying a potential lying in a direction to induce an electrical charge of conduction type opposite to a channel formed in a surface layer of the channel forming region of said TFT, in a lower portion of the channel forming region thereof to said body electrode and said back gate electrode so as to stabilize a threshold voltage of said TFT and increase a withstand voltage of the drain thereof.

However, Masuda, figures 1-44, and related text on col. 1-30, (figures 1-10), teach the step of applying a potential lying in a direction to induce an electrical charge of conduction type

opposite to a channel formed in a surface layer of the channel forming region of said TFT, in a lower portion of the channel forming region thereof to said body electrode and said back gate electrode so as to stabilize a threshold voltage of said TFT and increase a withstand voltage of the drain thereof.

Regarding claim 19, Numata, figures 1-51, and related text on col. 1-30, (figures 1, 44), disclose a method of driving a semiconductor device having a field effect transistor (FET) 1 formed in a semiconductor layer provided on an insulating layer 3, a body electrode 6 electrically connected to a channel 4 forming region of said TFT, and a back gate electrode 11 provided below the insulating layer 3 in an opposing relationship to the channel forming region of said TFT.

It is noted that Numata fails to teach the step of applying a potentials to the body electrode and the back gate electrode so as to increase threshold voltage of the TFT in an aging state for the semiconductor device.

However, Masuda, figures 1-44, and related text on col. 1-30, (figures 1-10), teach the step of applying a potentials to the body electrode and the back gate electrode so as to increase threshold voltage of the TFT in an aging state for the semiconductor device.

Regarding claim 20, Numata, figures 1-51, and related text on col. 1-30, (figures 1, 44), disclose a method of driving a semiconductor device having a field effect transistor (FET) 1 formed in a semiconductor layer provided on an insulating layer 3, a body electrode 6 electrically connected to a channel 4 forming region of said TFT, and a back gate electrode 11 provided below the insulating layer 3 in an opposing relationship to the channel forming region of said TFT.

It is noted that Numata fails to teach the step of applying potentials to the body electrode and the back gate electrode so as to increase threshold voltage of the TFT in a test state for measuring a leakage current.

However, Masuda, figures 1-44, and related text on col. 1-30, (figures 1-10), teach the step of applying potentials to the body electrode and the back gate electrode so as to increase threshold voltage of the TFT in a test state for measuring a leakage current.

Regarding claim 21, Numata, figures 1-51, and related text on col. 1-30, (figures 1, 44), disclose a method of driving a semiconductor device having a field effect transistor (FET) 1 formed in a semiconductor layer provided on an insulating layer 3, a body electrode 6 electrically connected to a channel 4 forming region of said TFT, and a back gate electrode 11 provided below the insulating layer 3 in an opposing relationship to the channel forming region of said TFT.

It is noted that Numata fails to teach the step of applying potentials to the body electrode and the back gate electrode which charge with time such that the threshold voltage of the TFT is increased or decreased in accordance with changes in time.

However, Masuda, figures 1-44, and related text on col. 1-30, (figures 1-10), teach the step of applying potentials to the body electrode and the back gate electrode which charge with time such that the threshold voltage of the TFT is increased or decreased in accordance with changes in time.

Regarding claim 22, Numata, figures 1-51, and related text on col. 1-30, (figures 1, 44), disclose a method of driving a semiconductor device having a field effect transistor (FET) 1 formed in a semiconductor layer provided on an insulating layer 3, a body electrode 6

electrically connected to a channel 4 forming region of said TFT, and a back gate electrode 11 provided below the insulating layer 3 in an opposing relationship to the channel forming region of said TFT.

It is noted that Numata fails to teach the step of applying potentials to the body electrode and the back gate electrode so as to increase threshold voltage of the TFT, wherein the TFT constitutes a predetermined circuit block, and activating another TFT constituting another circuit block at high speed in a state of being brought to a low threshold voltage.

However, Masuda, figures 1-44, and related text on col. 1-30, (figures 1-10), to teach the step of applying potentials to the body electrode and the back gate electrode so as to increase threshold voltage of the TFT, wherein the TFT constitutes a predetermined circuit block, and activating another TFT constituting another circuit block at high speed in a state of being brought to a low threshold voltage.

Regarding claim 23, Numata, figures 1-51, and related text on col. 1-30, (figures 1, 44), disclose a method of driving a semiconductor device having a field effect transistor (FET) 1 formed in a semiconductor layer provided on an insulating layer 3, a body electrode 6 electrically connected to a channel 4 forming region of said TFT, and a back gate electrode 11 provided below the insulating layer 3 in an opposing relationship to the channel forming region of said TFT.

It is noted that Numata fails to teach the step of applying potentials to the body electrode and the back gate electrode so as to increase threshold voltage of the TFT.

However, Masuda, figures 1-44, and related text on col. 1-30, (figures 1-10), to teach the step of applying potentials to the body electrode and the back gate electrode so as to increase threshold voltage of the TFT.

Regarding claim 31, Numata, figures 1-51, and related text on col. 1-30, (figures 1, 44), disclose a method of driving a semiconductor device having a field effect transistor (FET) 1 formed in a semiconductor layer provided on an insulating layer 3, a body electrode 6 electrically connected to a channel 4 forming region of said TFT, and a back gate electrode 11 provided below the insulating layer 3 in an opposing relationship to the channel forming region of said TFT.

It is noted that Numata fails to teach the steps of applying a first potential to the body electrode; and applying a second potential to the back gate electrode.

However, Masuda, figures 1-44, and related text on col. 1-30, (figures 1-10), teach the steps of applying a first potential to the body electrode; and applying a second potential to the back gate electrode.

Regarding claims 24-30, 32, see Numata, col. 1-30, and Masuda, col. 1-30.

It would have been obvious to one having ordinary skill in the art at the time of the present invention to apply the teachings of Numata into the method of Masuda as both are related to the same subject matter of fabricating a semiconductor device including a full depletion MISFET made by using a SOI layer and intended to stabilize a predetermined threshold voltage value.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Cricchi'894 is cited as of interest.

5. A shortened statutory period for response to this action is set to expired 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned

(see 710.02 (b)).

6. Any inquiry concerning this communication on earlier communications from the examiner should be directed to David Nhu , (703) 306- 5796. The examiner can normally be reached on Monday-Friday from 7:30 AM to 5:00 PM. The examiner's supervisor, David Nelms can be reached on (703) 308-4910.

The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956

David Nhu

March 19, 2003